REMARKS

The Remarks are in response to the Office Communication mailed on January 24, 2007, having a one-month, non-extendable response time. The Communication allowed all of the pending claims (claims 40, 47-51, and 53-57), but required compliance with the provisions of 37 CFR §41.202(a). As noted below for 37 CFR §41.202(a)(1), claims 40, 47-51, and 53-57 are either exact or close copies of claims from U.S. patent 6,538,926. It is noted that this information has largely been present previously, prior to the institution of 37 CFR §41.202(a)(1)-(6). An Office Communication mailed on August 17, 2004, also having a one-month non-extendable response period, required the corresponding information as part of a Request for Interference under the earlier rules.

Consequently, in response to the various portions of 37 CFR §41.202(a):

(1) Identification of Patent

Section (1) requires sufficient information to identify the patents with which the interference is sought.

Claims 40, 47-51, and 53-57 are respectively exact or close copies of claims 1, 8-12, and 14-18 of U.S. patent number 6,538,926 of Kato *et al.* granted March 25, 2003.

(2) Identification of Claims Believed to Interfere, Proposed Count, and Claim Correspondence

Section (2) requires that all claims believed to interfere are identified, that one or more counts is proposed, and that it is shown how the claims correspond to the one or more counts.

Claims 40, 47-51, and 53-57 are respectively exact or close copies of claims 1, 8-12, and 14-18 of U.S. patent number 6,538,926 and, consequently, so correspond. As all of these claims originate from the same patent, it is proposed that these claims could all be taken to correspond to a single count. Although the validity of this grouping has not been considered in detail, to facilitate the Interference process, the following is suggested.

Claim 40 of the present application, which is a close copy of claim 1 of U.S. patent number 6,538,926, is suggested as Count 1:

Count 1

> A nonvolatile memory system comprising:
> a nonvolatile memory including a plurality of nonvolatile memory cells and a buffer memory; and

a control device coupled to said nonvolatile memory, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,

wherein said nonvolatile memory is enabled to operate a program operation,

wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to said buffer memory and stores said data in said buffer memory to ones of said nonvolatile memory cells,

wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and

wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

Under the suggested grouping, claims 47-51 and 53-57 (and claims 8-12 and 14-18 of U.S. patent number 6,538,926) would also correspond to Count 1 under the suggested correspondence.

(3) Claim Chart for the Count

As the proposed Count 1 is Claim 40 of the present application, they correspond exactly:

Claim 40 of Present Application	Count 1
40. A nonvolatile memory system comprising:	40. A nonvolatile memory system comprising:
a nonvolatile memory including a plurality of nonvolatile memory cells and a buffer memory; and	a nonvolatile memory including a plurality of nonvolatile memory cells and a buffer memory; and
a control device coupled to said nonvolatile memory, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,	a control device coupled to said nonvolatile memory, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,
wherein said nonvolatile memory is enabled to operate a program operation,	wherein said nonvolatile memory is enabled to operate a program operation,
wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to said buffer	wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to said buffer

memory and stores said data in said buffer memory to ones of said nonvolatile memory cells,	memory and stores said data in said buffer memory to ones of said nonvolatile memory cells,
wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and	wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and
wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.	wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

The proposed Count 1 is a close copy of claim 1 of U.S. patent number 6,538,926 and so corresponds:

Claim 1 of U.S. patent number 6,538,926	Count 1
40. A nonvolatile memory system comprising:	40. A nonvolatile memory system comprising:
a nonvolatile memory including a plurality of nonvolatile memory cells and a buffer memory; and	a nonvolatile memory including a plurality of nonvolatile memory cells and a buffer memory; and
a control device coupled to said nonvolatile memory, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,	a control device coupled to said nonvolatile memory, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,
wherein said nonvolatile memory is enabled to operate a program operation,	wherein said nonvolatile memory is enabled to operate a program operation,
wherein in said program operation, said nonvolatile memory receives said data from said	wherein in said program operation, said nonvolatile memory receives said data from said

control device, stores said data to said buffer memory and stores said data in said buffer memory to ones of said nonvolatile memory cells,	control device, stores said data to said buffer memory and stores said data in said buffer memory to ones of said nonvolatile memory cells,
wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and	wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and
wherein said buffer memory has a data storing capacity enabling the receiving of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.	wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

Claim 1 of U.S. patent number 6,538,926 differs from the proposed Count 1 only in that the last element of Claim 1 of U.S. patent number 6,538,926 has "receiving" ("wherein said buffer memory has a data storing capacity enabling the receiving of a unit of data ...") instead of the "transfer" ("wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data ...") in Count 1. As "a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte" corresponds to "a data storing capacity enabling the receiving of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation", and the claims are otherwise the same, they consequently correspond.

As claim 40 of the present application and claim 1 of U.S. patent number 6,538,926 both correspond to Count 1 and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

(4) How Applicant Will prevail on Priority

As specified in the "Cross-Reference to Related Application" section, as amended by the Preliminary Amendment filed concurrently with the present application, of paragraph [0001] of the application, the present application is a continuation entitled to an effective filing date of July 26, 1991 due to the benefit of:

U.S. Application Serial No. 10/785,373, filed on February 23, 2004,

U.S. Application Serial No. 09/939,290, filed on August 22, 2001, now Patent No. 6,715,044,

U.S. Application Serial No. 09/657,369, filed on September 8, 2000, now Patent No. 6,317,812,

U.S. Application Serial No. 09/064,528, filed on April 21, 1998, now Patent No. 6,148,363,

U.S. Application Serial No. 08/931,193, filed on September 16, 1997, now Patent No. 5,806,070,

U.S. Application Serial No. 08/396,488, filed on March 2, 1995, now abandoned,

U.S. Application Serial No. 07/736,733, filed on July 26, 1991, now Patent No. 5,430,859.

U.S. patent number 6,538,926 is shown to have a United States filing date of October 31, 2001, claiming priority from a series of continuations and divisions back to U.S. Application Serial No. 08/164,780, filed on December 10, 1993, now Patent No. 5,592,415, which is a continuation-in-part of abandoned U.S. Application Serial No. 08/085,156, filed on July 2, 1993, and claims priority from a Japanese application filed July 6, 1992. The earliest of these U.S. applications is well over a year later than the July 26, 1991, effective filing date of the present application, with the Japanese application just under a year later than the July 26, 1991, effective filing date of the present application.

(5,6) Claim Charts

The following claim charts show the corresponding written description for each claim in the specification of the present application. They also show where the disclosure provides a constructive reduction to practice within the scope of the interfering subject matter.

Support for Claims

The pending claims of present application, including the proposed Count 1, are primarily concerned with the "Serial Protocol and Device" and "Controller Module" aspects of the present invention, primarily described in paragraphs [0072] and [0111] although additional details are provided in other sections. Particular attention is called to paragraphs [0095]-[0111].

The present application provides a number of differing embodiments and has a number of elements that can be taken as the "buffer memory" of the claims, such as elements 219 (Fig. 4), 337 (Fig. 6A), 413 (Fig. 7A), or 607 (Fig. 8B). Independent claims 40 and 51 differ from each other in that the first of these only has "a buffer memory", while claim 51 recites a plurality of nonvolatile memories *each* including a buffer memory. Although other embodiments are possible that recite a buffer memory, but not one for each of a plurality of memories, the same element (337) is referred to in the support for both of these independent claims.

References are to the clean version of the Substitute Specification submitted concurrently with the filing of the present application.

40. A nonvolatile memory system comprising: a nonvolatile memory including a plurality of nonvolatile memory cells and a buffer memory; and a control device coupled to said nonvolatile memory,	Memory system: 129 of Figs. 1A, 1B. Each memory module 131 contains one or more devices 141 [Figs. 2A, 2B] with cell array 201 [Fig. 4]. In one embodiment, element 337 [Fig. 6A] can be taken as the buffer. Controller: 133/134 of Fig. 1A/1B.
wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,	Figs. 1A, 1B., controller 133, 134 connected to outside of memory system along bus 123, 138.
wherein said nonvolatile memory is enabled to operate a program operation,	¶[0106]: "The microprocessor 121 then writes the R/W state machine 613 with a vector for a write command. The R/W state machine 613 selects the address registers 605 as the data source and enables the protocol state machine 623 to begin. ..."
wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to	¶[0081], lns. 5-6: "the information from the serial lines SI0, SI1 are now shifted into the enabled data shift register 337 and

said buffer memory and stores said data in said buffer memory to ones of said nonvolatile memory cells,	interpreted as data." ¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."
wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and	¶[0107]: "As data is shifted to the memory device the system microprocessor 121 [Fig. 1] continues to load data into the SERDES serial-parallel converter 607 [Fig. 8B] keeping data ready to be shifted to the memory device. ..."
wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.	In the terminology of the application, a chunk is unit of data stored in a program operation: "In the preferred embodiment, data is written and read in a 64-bit chunk." [¶[0093], ln.1] ¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."

The present application describes the structure of Flash EEPROM memory devices at paragraphs [0056]-[0058]. Many of the details are not explicitly recited in the present application, but are instead to be found in U.S. patents 5,172,338 and 5,297,148. Paragraph [0057] explicitly incorporates these patents by reference into the present application and, as such, they form an integral part of the present application.

47. A nonvolatile memory system according to claim 40, wherein said nonvolatile memory	See 141 Fig. 4, for an exemplary memory device including cell array 201. For the structure in terms of word lines and data

includes a plurality of word lines and a plurality of data lines, and wherein each of said nonvolatile memory cells is arranged at a crossing point of a corresponding one of said word lines and a corresponding one of said data lines and is coupled to the corresponding word line and corresponding data line.	lines, see, for example, U.S. patent 5,172,338, Fig. 4.

48. A nonvolatile memory system according to claim 47, wherein said nonvolatile memory includes a plurality of sectors each comprising one word line and ones of the nonvolatile memory cells coupled thereto, and wherein said buffer memory has a data storing capacity enabling the receiving of a unit of data of a length equal to the data storing capacity and enabling the storing of a unit of data in said sector.	On the structure of the memory (sectors, wordlines, cells), again see U.S. patent 5,172,338, especially beginning at col. 19, line 10. For the storing capacity of the buffer memory, see ¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."

49. A nonvolatile memory system according to claim 48, wherein said nonvolatile memory is a flash memory.	¶[0057]: "In the preferred embodiment, an array of flash electrically-erasable-programmable-read-only memories (EEPROM's) in the form of an integrated circuit chip is employed as the memory device 141. ..."

50. A nonvolatile memory system according to claim 40, wherein said control device includes	The control device can be taken as 133 (or 133 and 137) of Fig. 1A, with detail shown in Figs. 7A and 8A, or 134 of Fig. 1B,

a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memory and an external system bus.	with detail shown in Figs. 7B and 8B. In the first case, the recited elements can be taken as elements 411, 415, 417, 511, 543, 533. In the second case, elements 601, 605, 607, 611, 613, 615. The external system bus is123 (or 138).

51. A nonvolatile memory system comprising: a plurality of nonvolatile memories each including a plurality of nonvolatile memory cells and a buffer memory; and	Memory system: 129 of Figs. 1A, 1B. Each memory module 131 contains one or more devices 141 [Figs. 2A, 2B] with cell array 201 [Fig. 4]. In one embodiment, element 337 [Fig. 6A] can be taken as the buffer.
a control device coupled to said nonvolatile memories, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memories,	Controller: 133/134 of Fig. 1A/1B. Figs. 1A, 1B., controller 133, 134 connected to outside of memory system along bus 123, 138.
wherein said nonvolatile memories are enabled to operate a program operation,	¶[0106]: "The microprocessor 121 then writes the R/W state machine 613 with a vector for a write command. The R/W state machine 613 selects the address registers 605 as the data source and enables the protocol state machine 623 to begin. ..."
wherein in said program operation, each of said nonvolatile memories selectively receives said data from said control device, stores said data to said buffer memory thereof and stores said data in said buffer memory to ones of said nonvolatile memory cells of that	¶[0081], lns. 5-6: "the information from the serial lines SI0, SI1 are now shifted into the enabled data shift register 337 and interpreted as data." ¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data,

nonvolatile memory,	and outputs it in parallel on a WRITE data bus 347."
wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memories are operating in said program operation, and	¶[0107]: "As data is shifted to the memory device the system microprocessor 121 [Fig. 1] continues to load data into the SERDES serial-parallel converter 607 [Fig. 8B] keeping data ready to be shifted to the memory device. ..."
wherein said buffer memory has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.	In the terminology of the application, a chunk is unit of data stored in a program operation: "In the preferred embodiment, dta is written and read in a 64-bit chunk." [¶[0093], ln.1] ¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."

53. A nonvolatile memory system according to claim 51, wherein each of said nonvolatile memories further includes a plurality of word lines and a plurality of data lines, and wherein each of said nonvolatile memory cells in each of the nonvolatile memories is arranged at a crossing point of a corresponding one of said word lines and a corresponding one of said data lines and is coupled to said corresponding word line and corresponding data line.	See 141 Fig. 4, for an exemplary memory device including cell array 201. For the structure in terms of word lines and data lines, see, for example, U.S. patent 5,172,338, Fig. 4.

54. A nonvolatile memory system according to claim 53, wherein each of said nonvolatile memories includes a plurality of sectors each comprising one word line and ones of the nonvolatile memory cells coupled thereto, and	On the structure of the memory (sectors, wordlines, cells), again see U.S. patent 5,172,338, especially beginning at col. 19, line 10.
wherein said buffer memory has a data storing capacity for receiving data in units of a sector and enabling the storing of a unit of data in said sector.	For the storing capacity of the buffer memory, see ¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."

55. A nonvolatile memory system accordance to claim 54, wherein each of said nonvolatile memories is a flash memory.	¶[0057]: "In the preferred embodiment, an array of flash electrically-erasable-programmable-read-only memories (EEPROM's) in the form of an integrated circuit chip is employed as the memory device 141. ..."

56. A nonvolatile memory system according to claim 55, wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memories and an external system bus.	The control device can be taken as 133 (or 133 and 137) of Fig. 1A, with detail shown in Figs. 7A and 8A, or 134 of Fig. 1B, with detail shown in Figs. 7B and 8B. In the first case, the recited elements can be taken as elements 411, 415, 417, 511, 543, 533. In the second case, elements 601, 605, 607, 611, 613, 615. The external system bus is123 (or 138).

57. A nonvolatile memory system	The control device can be taken as

according to claim 51, wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the. nonvolatile memories and an external system bus.	133 (or 133 and 137) of Fig. 1A, with detail shown in Figs. 7A and 8A, or 134 of Fig. 1B, with detail shown in Figs. 7B and 8B. In the first case, the recited elements can be taken as elements 411, 415, 417, 511, 543, 533. In the second case, elements 601, 605, 607, 611, 613, 615. The external system bus is123 (or 138).

Conclusion

As presented above, it is respectfully submitted that the present application supports all of the currently pending claims and that the requirements of 37 CFR §41.202(a) have been met. A phone call to the undersigned is invited should there be any questions.

Respectfully submitted,

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2/26/07
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